PAPER VI: COMPUTER ORGANIZATION

Syllabus-Compliant Comprehensive Question Bank

UNIT I: Number Systems, Character Codes, Boolean Algebra, and Minimization

1 Mark Questions (Short Answer)

Q1. What is ASCII code and what is its standard bit-width?
Q2. Convert the decimal number 37 into its binary format.
Q3. Define a byte in digital computing terms.
Q4. What is the hexadecimal equivalent of binary 110111?
Q5. State the fundamental purpose of character codes like EBCDIC.
Q6. Write the boolean expression representing an exclusive-OR (XOR) gate.
Q7. Draw the truth table for a basic 2-input NAND gate.
Q8. State De Morgan's first theorem of Boolean algebra.
Q9. What logic function is performed by two inverted inputs fed into an AND gate?
Q10. What is a Karnaugh Map (K-Map)?
Q11. Define a Tri-State Buffer and its distinct three logic states.
Q12. Why are NAND and NOR gates categorized as universal gates?
Q13. What is the significance of the 'Don't Care' condition in a K-Map?
Q14. What does 'product-of-sums' (POS) form mean in logic systems?
Q15. State the duality principle in Boolean expression evaluation.
Q16. Write down the standard consensus theorem expression.
Q17. Define literal and minterm in the context of boolean logic.
Q18. What is the primary advantage of hexadecimal notation over binary strings?
Q19. Which character code can represent symbols from almost all international languages?
Q20. State the boolean simplification rule: A + A'B.

2 Mark Questions (Brief Explanations)

Q1. Differentiate between ASCII and EBCDIC character codes.
Q2. Convert the fractional decimal number 0.625 into its binary equivalent.
Q3. Explain the principle of the gray code and why it is useful.
Q4. Write down the truth table and standard logic symbol of a Tri-State Buffer.
Q5. Prove using a truth table that X + XY = X.
Q6. What is the law of absorption in Boolean algebra? Illustrate briefly.
Q7. Describe how an OR gate can be engineered using only NAND gates.

Q8. Explain how cells are adjacent in a 4-variable Karnaugh Map.

Q9. What are the structural benefits of minimizing a logic expression before circuit fabrication?

Q10. Explain the function of a high-impedance state in computer bus systems.

Q11. Convert the hexadecimal number 0x2AF3 into its decimal value.

Q12. What is the difference between standard form and canonical form of logic functions?

Q13. Draw the logic gate schematic for the expression Y = AB + C'.

Q14. How do you handle a 'Don't Care' condition when grouping cells in a K-Map?

Q15. Explain the concept of self-complementing codes with an example.

5 Mark Questions (Descriptive / Analytical)

Q1. Explain the decimal, binary, and hexadecimal number systems. Outline conversions between them.

Q2. State and prove both of De Morgan's Laws using truth tables and logic diagrams.

Q3. Minimize the given Boolean expression using algebraic theorems: F = A'B'C'D' + A'BC'D' + A'BCD' + A'B'CD'.

Q4. Simplify the following Boolean function using a 4-variable K-Map: F(A,B,C,D) = sum(0, 2, 5, 7, 8, 10, 13, 15).

Q5. Discuss the operational principles and hardware deployment of Tri-State Buffers in shared bus structures.

Q6. Demonstrate how any standard Boolean expression can be synthesized entirely using only NOR gates.

Q7. Explain the difference between gray codes and binary codes, highlighting binary-to-gray conversion steps.

Q8. Explain the structure, labeling, and grouping rules (pairs, quads, octets) of a 3-variable K-Map.

Q9. Reduce the following function to its minimal Sum of Products form: F(W,X,Y,Z) = sum(1, 3, 7, 11, 15) with don't cares d = sum(0, 2, 5).

Q10. Discuss basic electronic logic gates (AND, OR, NOT, XOR) including their truth tables, electronic symbols, and expressions.

8 Mark Questions (Comprehensive Long Essay)

Q1. Write an exhaustive guide on the minimization of combinational expressions. Compare the Boolean algebraic method against the Karnaugh Mapping technique, using a 4-variable logic function solved via both methodologies to prove identical outcomes.

Q2. Design a complete hardware logic framework that accepts a 4-bit binary input and produces a minimized output using a K-map. Synthesize the final circuit twice: first using only NAND gates, and second using only NOR gates. Provide complete schematic diagrams.

Q3. Explain the evolution, structure, and design of character coding standards from 7-bit ASCII to modern Unicode. Detail why bit-width expansions were essential for global operating systems and computing architectures.

Q4. Analyze the structural functionality and absolute necessity of Tri-State Buffers in multi-device bus-oriented digital computer layouts. Provide a full circuit diagram illustrating five peripherals sharing a common transmission line safely without signal collision.

Q5. Provide a rigorous proof of all fundamental axioms and theorems of Boolean Algebra (including Huntington's postulates, consensus, absorption, and Shannon's expansion). Demonstrate their immediate practical utility in decreasing logic gate propagation delays.

UNIT II: Combinational Circuits, Latches, Flip-Flops, Registers, and Counters

1 Mark Questions (Short Answer)

Q1. What is a combinational circuit?
Q2. Write down the Boolean expressions for the Sum and Carry of a Half Adder.
Q3. How many select lines are required for a 16-to-1 Multiplexer?
Q4. Define a decoder circuit.
Q5. What is the primary operational difference between a latch and a flip-flop?
Q6. Name the condition that makes an SR flip-flop unstable.
Q7. What does 'Master-Slave' configuration eliminate in a JK flip-flop?
Q8. Define edge-triggering in sequential systems.
Q9. What is the function of a T flip-flop?
Q10. What is a shift register?
Q11. How many flip-flops are needed to construct a counter up to modulo-16?
Q12. Define a synchronous counter.
Q13. What is the function of an encoder circuit?
Q14. What is Carry-Lookahead addition designed to speed up?
Q15. What does a bidirectional shift register do?
Q16. Define propagation delay in sequential circuits.
Q17. What is the state equation of a JK flip-flop?
Q18. State the difference between a ripple counter and a parallel counter.
Q19. What is a gated latch?
Q20. What is a universal shift register?

2 Mark Questions (Brief Explanations)

Q1. Differentiate between an encoder and a decoder circuit.
Q2. Draw the logic circuit diagram of a Half Adder.
Q3. Explain the racing or race-around condition in a JK flip-flop.
Q4. What are select lines in a multiplexer? Explain their routing mechanism.
Q5. Distinguish between synchronous and asynchronous sequential circuits.
Q6. Explain the clear and preset inputs of a flip-flop.
Q7. Describe how a D flip-flop can be constructed from an SR flip-flop.
Q8. Explain the basic configuration of a parallel-in, serial-out (PISO) shift register.
Q9. What is a ripple counter? Why is it called asynchronous?
Q10. Describe the purpose of the master-slave flip-flop setup.
Q11. Explain the role of lookahead carry generators in high-speed arithmetic logical units.
Q12. Show how a 2-to-4 decoder can be converted into a 1-to-4 demultiplexer.
Q13. What is an edge-triggered latch versus a level-triggered latch?

Q14. Define ring counter and state its sequence format.

Q15. Explain the state transitions of a basic T flip-flop.

5 Mark Questions (Descriptive / Analytical)

Q1. Design a Full Adder circuit using two Half Adders and an OR gate. Provide truth tables and logic diagrams.

Q2. Explain the design, truth table, and internal logic diagram of a 4-to-1 Multiplexer.

Q3. Explain the operation of a Master-Slave JK Flip-Flop. How does it resolve the race-around condition?

Q4. Design a 3-to-8 decoder with an enable input, providing its truth table and logic schematics.

Q5. Discuss the structure and operation of a 4-bit Binary Ripple Counter with sequential wave timing diagrams.

Q6. Describe the operation and distinct applications of four types of Shift Registers (SISO, SIPO, PISO, PIPO).

Q7. Explain the structural differences between Gated Latches and Edge-Triggered Flip-Flops with timing diagrams.

Q8. Design a Carry-Lookahead Adder unit for 4-bit additions, deriving the Boolean equations for propagates and generates.

Q9. Explain the operation, truth table, characteristic equation, and excitation table of a standard SR flip-flop.

Q10. Design a synchronous Mod-6 counter using JK flip-flops, detailing the state table and K-map simplifications.

8 Mark Questions (Comprehensive Long Essay)

Q1. Provide an exhaustive analysis of high-speed addition in digital processors. Derive the full carry-lookahead generation logic for a 4-bit block, illustrating how it minimizes propagation delay compared to a ripple-carry adder, and construct the full structural logic diagram.

Q2. Design and explain a comprehensive 4-bit synchronous up/down counter using JK Flip-Flops. Present the full state transition diagram, individual excitation tables, K-map minimizations for every single input, and the ultimate gate-level schematic.

Q3. Analyze the architectural problem of race-around conditions in level-triggered sequential systems. Provide a detailed structural breakdown of Master-Slave JK and Edge-Triggered Flip-Flops, outlining exactly how timing variations block feedback instabilities.

Q4. Design a multi-function 4-bit Universal Shift Register capable of holding data, shifting left, shifting right, and parallel loading. Provide the full internal circuit design utilizing multiplexers and D flip-flops, along with its control truth table.

Q5. Discuss the design methodology of large combinational subsystems. Demonstrate how to implement a 16-to-1 Multiplexer using a cascade of 4-to-1 Multiplexers, and explain how a priority encoder works with an explicitly solved 8-to-3 priority encoder case.

UNIT III: Basic Structure of Computers & Input/Output Organization

1 Mark Questions (Short Answer)

Q1. Name the main functional modules of a digital computer system.
Q2. What is the primary purpose of a system bus?
Q3. Define processor clock rate.
Q4. What is a multiprocessor computer system?
Q5. What is an interrupt service routine (ISR)?
Q6. Define Direct Memory Access (DMA).
Q7. What is a bus master?
Q8. What is the difference between a multiprocessor and a multicopter/multicomputer?
Q9. What does the acronym 'I/O' stand for in computer systems?
Q10. Define memory-mapped I/O mapping.
Q11. What is isolated or I/O-mapped I/O?
Q12. What is a cycle-stealing mechanism in DMA operations?
Q13. Name the register that holds the address of the next instruction to be fetched.
Q14. What is bus arbitration?
Q15. What is an interrupt vector?
Q16. Define execution time as a performance metric.
Q17. What is a standard I/O interface?
Q18. What is the purpose of the Accumulator register?
Q19. What is a daisy-chaining interrupt method?
Q20. Define program-controlled I/O transfer.

2 Mark Questions (Brief Explanations)

Q1. Differentiate between a multiprocessor system and a multi-computer network.
Q2. Explain the basic operational concept of a computer instruction cycle.
Q3. Describe the three main categories of lines found in a system bus structure.
Q4. Explain how performance is evaluated based on the basic computer performance equation.
Q5. What is an interrupt? How does the processor recognize it?
Q6. Explain the function of a DMA Controller inside a computer system.
Q7. Compare memory-mapped I/O with isolated I/O configurations.
Q8. What is an interface circuit? Why is it required between buses and I/O devices?
Q9. Explain the concept of central centralized bus arbitration.
Q10. Describe the purpose of the status register in an I/O interface circuit.
Q11. What is a vectored interrupt versus a non-vectored interrupt?
Q12. Explain the components of processor execution time.
Q13. What are the roles of MAR (Memory Address Register) and MDR (Memory Data Register)?
Q14. Describe the daisy chain priority mechanism for handling multiple interrupts.

Q15. What is a standard I/O bus? Give an example of a common interface standard.

5 Mark Questions (Descriptive / Analytical)

Q1. Discuss the functional modules of a digital computer system, describing how they interact during data processing.

Q2. Explain the structure and operation of a system bus, detailing data, address, and control lines.

Q3. Explain the mechanism of Direct Memory Access (DMA), highlighting the coordination between the CPU and the DMA controller.

Q4. Discuss the interrupt processing sequence in detail, from the device request to the completion of the Interrupt Service Routine (ISR).

Q5. Analyze the factors that influence computer performance based on the equation involving instruction count, CPI, and clock cycle time.

Q6. Compare program-controlled I/O, interrupt-initiated I/O, and direct memory access modes of data transfer.

Q7. Explain the architecture and working of a typical I/O interface circuit containing data registers, status registers, and control logic.

Q8. Discuss centralized and distributed bus arbitration schemes, outlining their respective pros and cons.

Q9. Describe the structural classification of computer types, distinguishing between workstations, mainframes, supercomputers, and embedded systems.

Q10. Explain standard I/O interfaces like PCI or USB, detailing their architectural benefits in modern computer systems.

8 Mark Questions (Comprehensive Long Essay)

Q1. Provide an exhaustive investigation into Input/Output data transfer mechanisms. Contrast Programmed I/O, Interrupt-Driven I/O, and Direct Memory Access (DMA) modes, and sketch a detailed timing sequence and structural diagram of a DMA-controlled block data transfer.

Q2. Explain the basic operational concepts of a computer. Draw the interconnected block diagram of a Von Neumann processor architecture, detailing every structural module, internal bus connection, register (PC, IR, MAR, MDR, AC), and trace a complete fetch-decode-execute instruction loop.

Q3. Analyze computer performance metrics thoroughly. Dissect the instruction performance equation: Time = N * CPI * T. Evaluate how microarchitectural changes, compiler optimizations, and semiconductor technological advancements directly affect each term.

Q4. Design a comprehensive architectural model for multi-device interrupt handling. Contrast Daisy Chaining, Polling, and Vectored Interrupt priority systems, evaluating how latency, hardware complexity, and extensibility scale across each approach.

Q5. Discuss multiprocessor and multi-computer architectures. Explain Flynn's taxonomy of computer systems (SISD, SIMD, MISD, MIMD), detailing how shared-memory multiprocessors handle inter-processor communication compared to message-passing multi-computer networks.

UNIT IV: Memory System, Cache Memories, and Virtual Memory Management

1 Mark Questions (Short Answer)

Q1. What is volatile memory?
Q2. Define static RAM (SRAM).
Q3. What is the main physical component used to store a bit in DRAM?
Q4. What does ROM stand for?
Q5. Define cache memory.
Q6. What is a cache hit?
Q7. What is a cache miss?
Q8. Define spatial locality of reference.
Q9. What is temporal locality of reference?
Q10. What is virtual memory?
Q11. What is a page fault?
Q12. Define hit ratio in memory hierarchies.
Q13. What is the purpose of a Memory Management Unit (MMU)?
Q14. Name a common secondary storage device.
Q15. What is flash memory?
Q16. What does EEPROM stand for?
Q17. What is cache mapping?
Q18. What is the write-through cache update policy?
Q19. Define memory latency.
Q20. What is a sector in a magnetic disk memory system?

2 Mark Questions (Brief Explanations)

Q1. Differentiate between Static RAM (SRAM) and Dynamic RAM (DRAM).
Q2. Explain the trade-offs between memory speed, size, and cost across the memory hierarchy.
Q3. Describe the basic operation of a Read-Only Memory (ROM) cell.
Q4. Explain the principle of Locality of Reference and its impact on cache utilization.
Q5. What is direct cache mapping? Briefly outline its indexing layout.
Q6. Explain the write-back policy used in cache memory consistency systems.
Q7. What is virtual memory? Why is it beneficial to software execution?
Q8. Explain page tables and their role in virtual-to-physical address translation.
Q9. Describe the function of a Translation Lookaside Buffer (TLB).
Q10. What is the difference between a page and a frame in virtual memory management?
Q11. Explain the seek time and rotational latency parameters of a magnetic secondary disk storage device.
Q12. Describe the basic architecture of a semi-conductor RAM memory array.
Q13. What is a page replacement algorithm? Name two common variants.

Q14. Explain the performance considerations when designing a two-level cache system.

Q15. What are the primary memory management requirements of modern multi-tasking operating systems?

5 Mark Questions (Descriptive / Analytical)

Q1. Discuss the computer memory hierarchy, explaining how speed, size, and cost considerations mandate a multi-level storage architecture.

Q2. Explain the internal structure and working principles of Static RAM (SRAM) and Dynamic RAM (DRAM) memory cells.

Q3. Describe cache memory principles, explaining how temporal and spatial locality of reference enable high hit ratios.

Q4. Explain the direct mapping cache organization technique, highlighting address fields and mapping mechanics.

Q5. Discuss associative mapping and block-set-associative mapping techniques used in cache organizations with structural diagrams.

Q6. Explain the concept of Virtual Memory using a paging mechanism, detailing how a logical address is converted into a physical address.

Q7. Describe the page fault handling routine step-by-step when a requested page is absent from main memory.

Q8. Discuss the performance considerations of cache memory, deriving an expression for average memory access time based on hit ratio.

Q9. Explain the hardware architecture, types, and programming requirements of Read-Only Memories (ROM, PROM, EPROM, EEPROM, Flash).

Q10. Discuss secondary storage technologies, detailing the physical data organization (tracks, sectors, cylinders) of magnetic disk systems.

8 Mark Questions (Comprehensive Long Essay)

Q1. Provide an extensive architectural assessment of Cache Memory Mapping Strategies. Contrast Direct Mapping, Fully Associative Mapping, and Set-Associative Mapping configurations, providing full schematic layout block diagrams, address split models, and tracking memory access strings.

Q2. Design a comprehensive virtual memory management framework utilizing a paging model. Explain the entire address translation pipeline from a CPU-generated virtual address to a physical main memory address, detailing the internal operations of the MMU, Page Table, TLB cache, and page fault resolution workflows.

Q3. Analyze semiconductor random access memories. Sketch the transistor-level structural circuit diagram of a 6-transistor SRAM cell and a 1-transistor DRAM cell, evaluating their operational mechanics, refresh requirements, power dissipation factors, and integration densities.

Q4. Discuss the multi-tiered memory system configuration of a modern digital computer. Evaluate how speed, capacity, and cost metrics are optimized globally through registers, L1/L2/L3 caches, primary RAM arrays, and secondary non-volatile magnetic/solid-state storage, using explicit performance calculations.

Q5. Write a comprehensive research report on Memory Management Requirements in concurrent computing systems. Explain memory protection bounds, dynamic relocation, sharing, swapping, fragmentation challenges, and the detailed execution of the Least Recently Used (LRU) page replacement algorithm.